An Area-Efficient Architecture for Stochastic LDPC Decoder

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***Abstract*—Stochastic computation is an excellent approach for low-density parity-check codes decoding. By adding edge memories at each edge in the Tanner graph, fully parallel hardware implementation can be designed with much lower wire complexity. This feature can alleviate the wire congestion in conventional Min-Sum decoders. However, edge memories occupy large physical area percentage of variable node and cause large dynamic power dissipation. In this paper, we propose an area-efficient counter based structure for variable nodes. In order to reduce the area of variable nodes, we eliminate the edge memories in all variable nodes and reuse the counter designed to function the hard-decision to trace the probability of the prior message. The value boundary of the counter is enlarged to record the probability more precisely, and the value of the counter is compared with a random number to determine the output of variable nodes. We also reuse parts of some sub-units in variable nodes to build others. As a result, for LDPC codes of 10GBASE-T (IEEE 802.3an-2006), the proposed structure of variable node can reduce 88.3% EM based variable node area.**

***Index Terms*—low-density parity-check codes; stochastic computation; area-efficient; counter based**

I. Introduction

Low-density parity-check (LDPC) codes are outstanding linear block codes which can achieve excellent performance close to the Shannon limit. LDPC codes were invented by Gallager in 1962 [1], and rediscovered by Mackey and Neal in 1997 [2]. LDPC codes are used widely in several communication standards owing to the excellent performance.

Like other linear block codes, the parity check matrix (PCM) is used to illustrate the LDPC codes. Tanner graph can show the architecture of LDPC decoder more clearly. Tanner graph expresses the row of PCM as check node (CN), and the column of PCM as variable node (VN). If the corresponding element in the PCM is 1, an edge is connected between the CN and VN. Based on the Tanner graph, some message-passing algorithms including Sum-Product Algorithm (SPA) and Min-Sum Algorithm (MSA) are used to decode the LDPC codes. In these algorithms, the CNs and VNs calculate the received soft messages and exchange the results through the edges. SPA and MSA can achieve better decoding performance, but the hardware complexity prevents the LDPC decoder to obtain a further performance development.

Stochastic decoding is deduced from SPA which is calculated in the probability-domain [3]. The probability values from the channel are represented as streams of Bernoulli sequences. The mathematical expectation of the 1s in the stream of Bernoulli sequences is equal to the channel probability. Therefore, stochastic decoding is a kind of bit-serial algorithm can reduce the routing congestion of SPA and MSA.

However, because of the girth in the Tanner graph, the outputs of stochastic LDPC decoder may stay at a fixed state, resulting in latching problem. In order to mitigate this problem, the concept of edge memories (EMs) was proposed in [4]. EMs are added at each edge of the Tanner graph and used to trace the prior probability of the outputs of VNs. The decoders based on EMs can enhance the accuracy of decoding significantly. However, EMs occupy too much area of VNs and cause large dynamic power dissipation.

In this paper, we propose an area-efficient stochastic LDPC decoder architecture which is based on counters. By implementing an LDPC decoder which can decodes the code from IEEE 802.3an (10GBASE-T) [5], we show that this new architecture can achieve small VN area with little performance loss. According to the feature of the LDPC codes for the IEEE 802.3an standard, we also reuse some parts of VN to reduce some area of VN too.

The remainder of this paper is organized as follows. Section II gives an overview of decoder architecture based on EMs. Section III presents the new VN structure based on counter. Results of simulations and synthesis are showed in Section IV. Finally, conclusions are given in Section V.

II. Review of the Decoder Architecture Based on EMs

The architecture of a stochastic decoder is based on Tanner graph. The VNs and CNs are connected to each other and transmit messages on the edges. The EMs are located at the edges in the VNs. The EM consists of a shifting register and a net of multiplexers. By using the multiplexers, bits in EM can be selected randomly. The random number is generated by Linear Feedback Shift Registers (LFSRs).

The function of the VNs is to check the inputs are whether the same or not. Fig.1 shows the structure of 2-inputs VN based on EM presented in [4]. The VNs receive the Bernoulli sequences from the channel and the prior messages from the connected CNs, one bit in each decoding cycle (DC). If the

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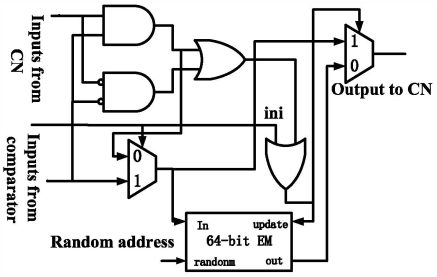

Fig. 1. The structure of 2-inputs VN which based on EM

channel bit and the prior message bit are the same, the VN is in the unhold state. In this state, VN outputs the channel bit directly to corresponding CNs and input this bit to EM. On the contrary, if the channel bit and the prior message bit are different, the VN is in the hold state and VN has to find other messages to output. Because the bits in EM are unhold bits in previous DCs and the probability of 1s in EM can represent the probability of the unhold sequence, the VN will select a bit randomly from EM as the output when it is in the hold state.

The function of the CN is to check whether the inputs satisfy the check equations of PCM. Because of the stochastic decoding and bit-serial feature, the structure of CN is a sample net of XOR gates. Except for VNs and CNs, the stochastic decoder also needs a block to convert the messages from channel to probability. The probability can be computed by (1):

$$P_i = \frac{e^{L_i}}{e^{L_i} + 1} \tag{1}$$

where the L_i is the channel log-likelihood ratio (LLR). Look Up Tables (LUTs) are used to calculate the probability, and noise dependent scaling (NDS) technology [4] is used to limit the channel messages in an appropriate range.

The hard-decision of the decoder is calculated by a saturated up/down counter is VN. The value of counter is range from +7 and -7 and the sign bit of the value determines the hard-decision.

III. THE NEW STRUCTURE OF VN

Although adding EMs to VN can mitigate the latching problem and the stochastic decoder based on EMs can achieve excellent performance, EMs still have a lot of problems. The LDPC code used in this paper is the (2048, 1723) code adopted in the 10GBASE-T standard. The PCM of this codes is a regular matrix, which means the number of 1 in each row or column is the same. The degree of the CN is 32 and the VN is 6. So each VN contains six sub-units to connect six CNs. A fully parallel stochastic LDPC decoder for (2048, 1723) code has 12288 edges, so it has 12288 EMs too. That will occupy a large area of a decoder. For example, VNs occupy about 75% area of the whole decoder and the 64-bit EMs occupy a large part of VN, about 80%, so about 60% physical area of a decoder are the EMs, which causing area waste and high dynamic power dissipation.

The function of EM is a probability tracer for outputs of the unhold state. When a VN is in the unhold state, the EM is updated with the input from comparator which convert the channel probability to Bernoulli sequences. Here the updated means the input is shifted into the EM and the most significant bit (MSB) is shifted out. EMs remain the same when the VNs are in the hold state. Therefore, after several DCs, EM will be full of unhold bits and the probability of unhold sequences is approximately equal to the mathematical expectation of EM bits. That means, the outputs of VN when it is in hold state follow actually the unhold state's outputs.

The saturated up/down counter is a good choice to replace the EM [4]. If input a 1 to EM, the counter value increases 1, and if input a 0 to EM, the counter value decreases 1. As a consequence, the value of counter can express the probability of outputs when the VN is at the unhold state. The hardware consumption of a counter is much less than an EM. For example, a 64-bit EM needs 64 registers, while a counter which saturated value is 128 needs 7 registers only. Just like EM, when VN is at hold state, the value of counter is compared to a random number which is created by LFSR [6]. If the value of counter is larger than the random number, the output of VN is 1 and otherwise 0.

In the VN structure based on EM, there are six EMs in one VN and each sub-units have one EM. In fact, the functions of each sub-unit are the same, the probabilities of the six probability tracers are close and only the inputs from CNs are different. Therefore, only one probability tracer can fulfill the function of six probability tracers, which will save a large hardware consumption.

The hard-decision output of one VN is generated by a saturated up/down counter. The outputs of each VN are sent to correspondent saturated up/down counter and the inverse MSB of the counters value is outputted as the hard-decision. The probability tracer of the VN is also an saturated up/down counter and after scaling, one VN has one probability tracer now. The operation of hard-decision counters and probability tracer are the same, so the probability tracing saturated up/down counter can be reused as hard-decision saturated up/down counter. Fig. 2 shows the block graph of the counter in the proposed VN.

Fig. 3 shows the structure of a 6-inputs sub-unit. The internal memory (IM) is a kind of short EM which used in the sub-unit to improve the performance. The sub-unit receives one input

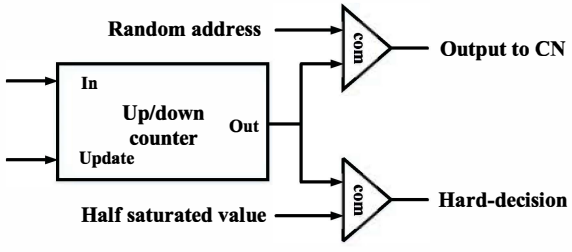

Fig. 2. Up/down counter in VN

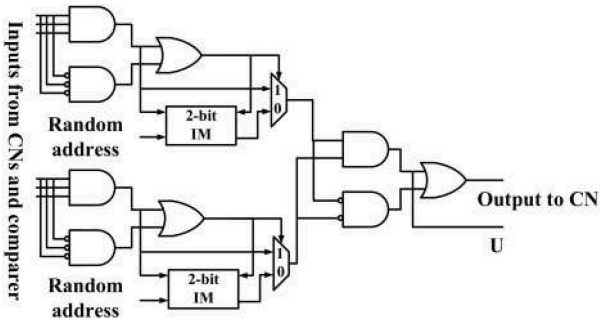

Fig. 3. Structure of a 6-inputs sub-unit

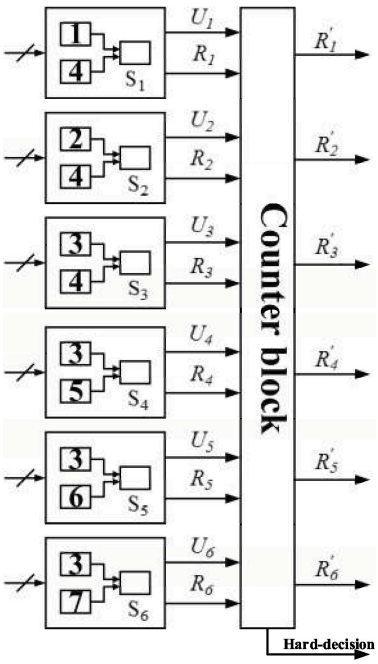

Fig. 4. The block graph of VN based on counter

from the comparator and five inputs from CNs except the CN which receives the output of this sub-unit. Although the inputs are different, the structure of the six sub-units are the same. The six inputs of a sub-unit are divided into two groups, each group contains 3 inputs. The 3 inputs of each group are checked first and get intermediate results, then a 2-inputs group checks the two intermediate results and get the final result. Therefore, six sub-units have 12 3-input groups. Table I lists the inputs of each sub-unit in detail and the number in the bracket represents the number of inputs group. Table I shows that the 12 3-input groups actually only contains 7 different kinds of groups, so the structure can be reduced by reusing certain 3-inputs groups to construct the whole sub-units. Fig. 4 represents the block of VN based on counter. The numbers in each sub-unit means it contains the corresponding group in Table I. The counter block contains the saturated up/down counters in Fig. 4 and six multiplexers to determine the outputs. The output to the CN equals to the output of sub-unit if the correspondent U signal is high and on the other

TABLE I
THE INPUTS DISTRIBUTION OF EACH SUB-UNITS

sub-units in VN	The source of inputs of each sub-unit (From CNs and comparator)	
	The first group	The second group
S_1	C_2,C_3,comparator(1)	C_4,C_5,C_6(4)
S_2	C_1,C_3,comparator(2)	C_4,C_5,C_6(4)
S_3	C_1,C_2,comparator(3)	C_4,C_5,C_6(4)
S_4	C_1,C_2,comparator(3)	C_3,C_5,C_6(5)
S_5	C_1,C_2,comparator(3)	C_3,C_4,C_6(6)
S_6	C_1,C_2,comparator(3)	C_3,C_4,C_5(7)

hand, it equals to the output of counter if the U signal is low. When the U signals of all sub-units are high, the outputs of sub-unit are sent to counter and the counters value is updated.

IV. RESULT

Fig. 5 shows the block graph of the whole architecture of the decoder. The LFSR block contains 64 LFSRs [7], so every 32 VNs share one LFSR. The termination criteria of this decoder is 700 DCs and the terminal signal is generated by Check block which has a similar structure to the CN block.

A. Bit-Error-Rate performance

Fig. 6 represents the comparison of the Bit-Error-Rate (BER) performance of the proposed stochastic decoder and other LDPC decoders. The LDPC codes used in this paper is the (2048, 1723) codes which is chosen from IEEE 802.3an (10GBASE-T). Three different proposed decoders are showed in the BER graph, the saturated values of the three counters are 64, 127 and 255 and the depthes of the three counters are 6-bit, 7-bit and 8-bit, respectively. For comparison, Fig. 6 also shows the performance of decoder based on 64-bit EM and float Min-Sum decoders. All message from the channel are quantized to 6 bit including 1 sign bit, 2 integer bits and 3 decimal bits. Fig. 6 shows that the performance of all proposed decoders are better than 64-bit EM.

B. Comparison results

In order to compare the hardware area of proposed 7-bit counter decoder and the decoder based on EM, the decoders are synthesized in SMIC 65nm 1.0V by using Design Compile

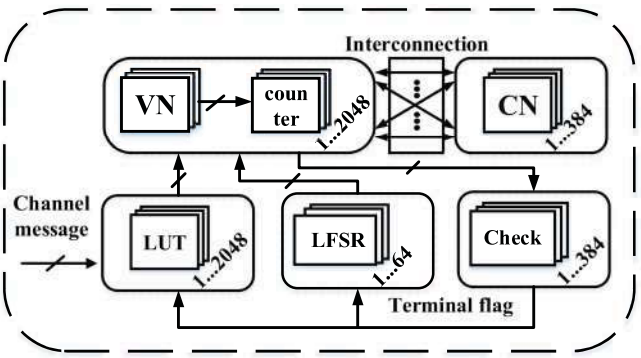

Fig. 5. The block graph of proposed decoder

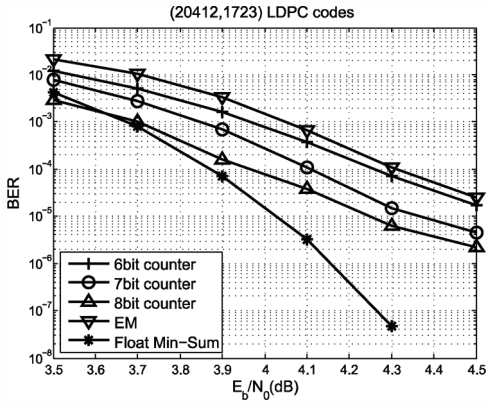

Fig. 6. The BER performance for (2048,1723) codes

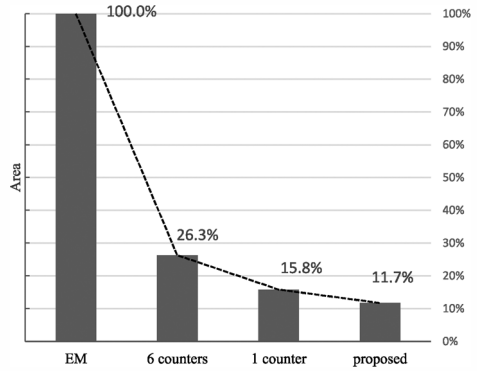

Fig. 7. Reduction in area by using proposed methods

TABLE II
SYNTHESIS RESULTS OF VNS IN SMIC 65NM 1.0V

	Area of VN (um^2)	Area of counter or EM (um^2)	Ratio of probability tracer and VN
Proposed VN	827.6	257.0	31.1%
1 counter VN	1110.2	257.0	23.2%
6 counters VN	1855.8	1818.7	98.0%
EM-based VN	7044.1	5863.2	83.2%
TFM VN [10]	2773.9	-	-
MTFM VN [6]	1005.1	-	-

of Synopsys. The area of VN and the probability tracer are detailed in Table II. The 1-counter VN means the 6 sub-units in one VN share one counter and the 6-counters VN means each sub-unit contains a counter. Fig. 7 shows the reduction in area after using the proposed methods. Compared to EM-based VN , the counter-base VN can achieve significant area reduction. Table II also shows the area of the proposed decoder requires about 29.8% and 82.3% area of TFM and MTFM, respectively.

Table III compares the area and power consumption of the whole decoder based on counter, EM and others. The decoders are all scaling to 65nm. Table III shows that decoder based on counter only require 15.3% area of decoder based on EM, and smaller than MTFM [6],RHS [8] [9], too.

At the SNR of 5.5dB, the decoder based on 7-bit counter can decode one code word in average 100.4 DCs and the throughput is 10.2 Gb/s.

TABLE III
SYNTHESIS RESULTS OF DECODER IN SMIC 65NM 1.0V

	Area (mm^2)	Frequency (MHz)	Throughput (Gb/s)
proposed	2.2	500	10.2
EM [6]	14.4	500	-
MTFM [6]	3.3	500	61.3
[8]	4.4	448	160
[11]	7.6	207	5.3

V. Conclusion

We have presnted an area-efficient architecture for stochastic LDPC decoder. Saturated up/down counter is used as probability tracer in VNs and some parts of sub-units in VN are reused. The proposed decoder is synthesized in SMIC 65nm 1.0V at 500MHz for the LDPC code in 10GBASE-T. Compared to the decoder based on EMs, the chip area is reduced about 15.3% and the decoder achieve 10.02 Gb/s at the SNR of 5.5dB.

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