A High-Throughput LDPC decoder For Optical Communication

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Abstract

As Optical Communication is on the way, conventional LDPC decoders do not work well with the requirement for high throughput over 100 Gb/s. Many new LDPC decoder structures aiming at high throughput have been proposed, such as stochastic decoders, bit serial decoders, digit serial decoders and so forth. In this paper, a Min-Sum fully parallel structure using clock multiplexing is proposed, as an attempt to relieve the wiring problem. This decoder makes full use of clock edges comparing to conventional decoders. With SIMC 0.13um technology, our decoder achieves a throughput of 54.2 Gb/s at 200MHz for the WiMAX standard of 5/6 code rate. Our conjecture is that with lower feature size and higher clock frequency, 100 Gb/s could be achieved.

Keywords: LDPC, high throughput, clock multiplexing.

1. Introduction

Since Low-Density Parity-Check (LDPC) codes was proposed by Gallager [1], LDPC codes have been widely applied in all varieties of communication standards as it was proved to outperform Turbo code to get close to the Shannon Limit.

In recent years, there is a lot of work on the high throughput standards, such as 10Gbase-T, WiMAX, etc. for optical communication. In order to achieve ultra-high throughput, many different types of decoders are proposed. Bit serial decoder buffers all data values in parallel [2], and asks for an extra frame interleaving. Digit serial decoder in [3] uses deep pipeline to achieve a throughput of 42.7 Gb/s with 10 bits LLR precision, but introduces an ultra-high clock frequency of 2 GHz. Stochastic decoder requires fewer wires than conventional decoders, but does not get a desirable coding gain [4]. Modified partially parallel decoders are also proposed [5], and perform well.

As to fully parallel LDPC decoders, some early structures are presented, such as Macro-Layer Level decoder [6], LUT-based decoder [7]. The main problem of fully parallel LDPC decoder is wiring congestion. As the parallelism of a bit-parallel message-passing decoder increases, the wiring overhead increases [5] enormously. To solve this problem, wiring partitioning is used in [8], which of course increase the chip area. And the clockless decoder with asynchronous interleaver [9] can achieve an uncoded throughput of 46 Gb/s. In this paper, clock multiplexing is proposed, which can address wiring congestion and double the throughput of conventional fully parallel LDPC decoders at the same time.

In section 2, Min-Sum Algorithm is briefly introduced, and the quantization scheme and BER performance are given. In section 3, the proposed architecture is described in detail. In section 4, an analysis of throughput, area, clock frequency is presented. In section 5, a conclusion is drawn.

2. Algorithm

Our proposed decoder chooses the Normalized Min-Sum Algorithm, which reduces hardware complexity substantially in comparison with the Sum-Product Algorithm, at the cost of the degrading of BER curve, which consequently is still reliable [10].

The decoding steps are shown below:

Step 1) Initialize:

Receive intrinsic information from channel as INTR, and set LLRs as a proportion to INTR.

Step 2) Check Nodes update:

Calculate the information from Check Nodes to Variable Nodes, R, with Equation (1) below.

$$R_{mn} = \alpha \bullet \prod_{n' \in N(m)/n} sign(L_{mn'}) \bullet (\min_{n' \in N(m)/n} | L_{mn'} |) \quad (1)$$

α is the scaling factor. R_{mn} denotes the information from Variable Node m to Check Node n.

Step 3) Variable Nodes update:

Calculate the information from Variable Nodes to Check Nodes, L, with Equation (2).

$$L_{mn} = I_n + \sum_{m' \in M(n)/m} R_{m'n} \quad (2)$$

Step 4) Iteration Stop:

Calculate the posterior message with Equation (3).

$$S_n = I_n + \sum_{m \in M(n)} R_{mn} \quad (3)$$

Then execute Hard Decision with Equation (4).

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$$x_n = \begin{cases} 1, & S_n < 0 \\ 0, & S_n \geq 0 \end{cases} \quad (4)$$

If $\{x_n\}$ satisfies Equation (5), decoding succeeds and iteration is terminated. Otherwise, it goes back to **step 2**. H represents the Parity Check Matrix.

$$x_n \bullet H^T = 0 \quad (5)$$

Following Figure 1 shows the float point BER curves for standard WiMAX of code rate 5/6 with different scaling factors.

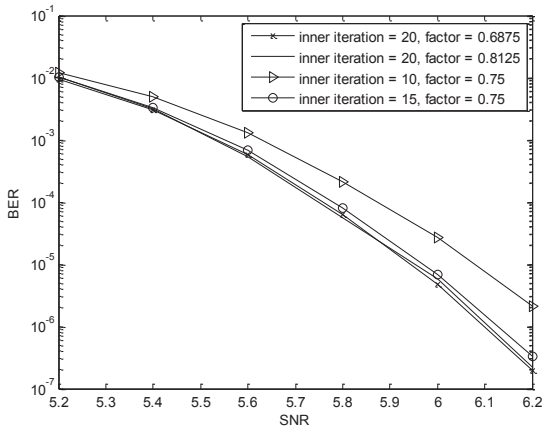

Figure 1. Float Point BER under different max iteration numbers and scaling factors

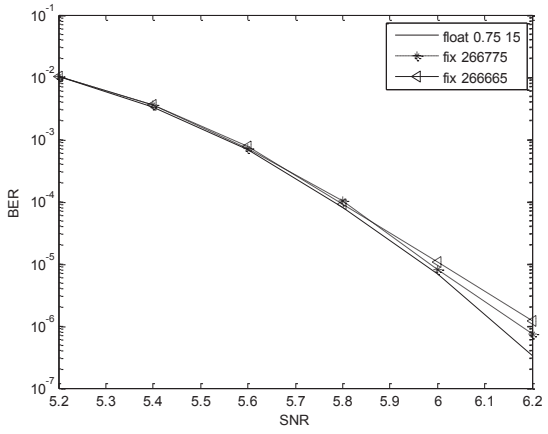

Figure 2.Fixed Point BER with max iteration number 15

In the proposed design, max iteration number is 15, as shown in Figure 2, and the quantization scheme is 26666 with little coding gain loss compared with float point. The quantization scheme of 26666 means that INTR, L, R and S are 6-bit messages, each including a 2-bit fraction. In Figure 2, no error floor occurs, which is of great significance in Optical Communication.

3. Architecture

A. Fully Parallel Structure

In fully parallel LDPC decoders, messages from all nodes of the same kind is processed simultaneously, which could increase the throughput enormously. And in comparison with partially parallel decoders, proposed design need less memory.

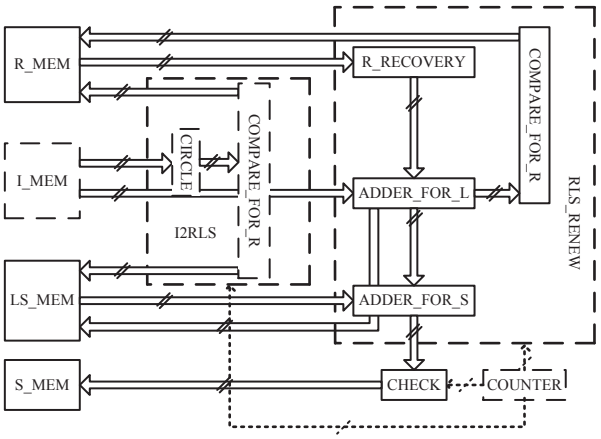

Figure 3.Fully Parallel LDPC decoder structure

System structure is shown in Figure 3. I_MEM is the intrinsic information memory. LS_MEM is the memory for L in step 3, but here we just store the sign bits. For 6-bit quantization LLR memory, proposed decoders can save 5/6 compared with layered decoding [11]. R_MEM stores R, including 16bits in a unit. For example, R[15:0] includes a 5-bit minimum of corresponding LLRs, a 5-bit second minimum of corresponding LLRs, a 5-bit location indicating the position of minimum and the product of the sign bits of corresponding LLRs. S_MEM stores the decoding results. I2RLS, RLS_RENEW and CHECK blocks are combinational modules that can proceed from step 2 to step 4. Four-bit COUNTER tells the number of iteration. Only when COUNTER is 0, I2RLS is active. And only when COUNTER is 15, decoding result is stored into S_MEM.

Proposed design integrates the R and L update in one block, so in every single clock cycle, the decoder calculates new R and L in the meantime.

Intrinsic information first goes to the CIRCLE, and is shifted according to the parity check matrix, initializing LLRs. Then LLRs are compared to get R. After the above initialization, L and R are used to calculate new information in different iteration in RLS_RENEW. In RLS_RENEW, R_RECOVERY, ADDER_FOR_R/L and

COMPARE_FOR_R blocks are adopted. In each cycle, code is checked. Code will be stored only when decoding succeeds or ends, which reduces the power consumption.

B. Clock Multiplexing

Conventional design only uses one edge of the system clock, to achieve ultra-high throughputs. Proposed decoder doubles the whole memory, naming them MEM0 and MEM1. MEM0 is sensitive to the positive edge of clock, while MEM1 is sensitive to the negative edge. But the two memory systems share the same combinational blocks, I2RLS and RLS_RENEW. Proposed decoder generates an ACTIVE signal to indicate which memory of the two should use the combinational blocks and where does the forthcoming data go. ACTIVE signal is 0 if MEM0 is working. ACTIVE signal is 1 if MEM1 is working. The data flows as Figure 4 shows.

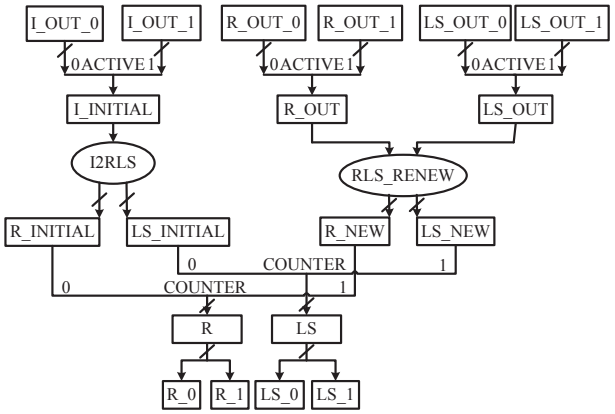

Figure 4. Proposed data flow

I_OUT_X, R_OUT_X and LS_OUT_X present the output of I_MEM, R_MEM and LS_MEM respectively. R_X and LS_X are the input of R_MEM and LS_MEM. Here X equals to 0 or 1. When COUNTER is 0, R_INITIAL from intrinsic information is stored. If COUNTER is not 0, R_NEW from RLS_RENEW block is stored. And same for the LLRs.

In fact, when a clock edge comes, information of code_0 in the combinational blocks is stored into MEM_1 and vice versa. So clock frequency must be precisely controlled to satisfy proper time constrains.

C. Block Design

In the combinational blocks, to reduce the wiring congestion and flatten the latency, several blocks are proposed. CIRCLE block is designed to function like the Barrel Shifter. COMPARE block is designed to compare LLRs to get new R information. R_RECOVER block is for recover the entire R information from the reduced R_MEM. R_RECOVER is shown in Figure 5. R_REST denotes the rest bits of R besides the sign bit.

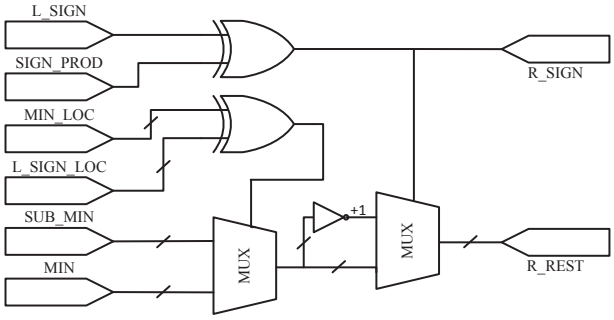

Figure 5.R_RECOVER block

4. Analysis

A. Throughput

Proposed decoder takes advantage of both two edges of clock signal, obviously doubling the throughput of conventional fully parallel LDPC decoders. With proper arrangement of timing, two codes could be decoded in one decoding cycle, and received in turn at the positive and negative edge of clock respectively.

Design Compiler reports that the throughput of proposed decoder of SMIC 0.13um technology is 54.2 Gb/s at 200MHz, as shown in Table 1.

A design for the (2048,1723) 10Gbase-T LDPC code in 90nm at 250MHz was proposed in [12] and a partially parallel design for the (2048,1723) 10Gbase-T LDPC code in 65nm at 700MHz in [13].

Table 1. Design Comparison

	[12]	[13]	Proposed
Technology	90nm	65nm	0.13um
Clock	250MHz	700MHz	200MHz
Throughput	16Gb/s	47.7Gb/s	54.2 Gb/s
Area	9.8mm2	5.35mm2	57.6 mm2
Scaled Area in 65nm CMOS	5.1mm2	5.35mm2	14.4 mm2
ACE	1.254	1.274	1.881
Power@5.5dB	1.383W	2.80W	NA

Also we define the Area Clock Frequency Efficiency (ACE) as throughput/area/clock frequency. As the clock frequency is related to the power consumption, ACE is a proper parameter for measuring chip throughput efficiency for designs after synthesis. In Table 1, proposed design achieves the highest ACE as 1.881. In Table 1, power consumption in [12] and [13] are 1.383W and 2.8W respectively. The super high power consumption problem still remains in proposed design, and further improvement is required.

B. Area

As presented in [14], the size of fully parallel decoder is determined by the wiring congestion, but not logic area. In this design, two memory systems sharing the

same combinational blocks, will apparently subtract a certain amount of area from that of two chips, providing a new method for other high throughput designs. The area in Table 1 is given by Design Compiler.

C. Clock Frequency

In this design, clock frequency is set to 200MHz in SMIC 0.13um technology. If it is done in 65nm technology, a higher clock frequency, approximately 400MHz, can be adapted, and a throughput of 108.4 Gb/s can be achieved, satisfying the requirement of Optical Communication. Compared with other high-throughput designs, the requirement for high clock frequency of proposed design with fully parallel structure is not that strict, which seems to reduce the power consumption.

5. Summary

In this paper, a high-throughput LDPC decoder with fully parallel structure via clock multiplexing is proposed, to meet the requirement of Optical Communication for over 100 Gb/s. This structure could be adopted by other designs to trade off area for throughput. In fact it is not a merely tradeoff but an improvement, because the wiring congestion is relieved.

Acknowledgments

This work is supported by the National Natural Science Foundation of China (Grant No.61306043)，the Shanghai Natural Science funding (Grant No.13ZR1401800).National Science and Technology Major Project of China (Grant No. 2011ZX03003-003-03), the Science and Technology Foundation of State Key Laboratory of ASIC & system (Grant No.11ZD0005), “Dawn” Program of Shanghai Education Commission (Grant No,11SG07).

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